REMARKS

Claims 1-35 have been presented and pending for examination, and all have been rejected under 35 U.S.C. § 112 or 103. Claims 1, 6, 11, 13, 18, 21, 23, 28, and 31 are being amended. In view of the above amendments and following remarks, withdrawal of the rejections and reconsideration of the application are respectfully requested.

CLAIM REJECTIONS UNDER 35 U.S.C. § 112 First Paragraph

In paragraph 3 and 4 of the above-mentioned Final Office Action, claims 1-35 were rejected under 35 U.S.C. § 112, first paragraph because "realistic time" was not "described in the Specification," "[i]t is unclear what the limitation of 'realistic time' is referring to" and "[s]pecifically, no definition has been given to 'realistic time'". It is respectfully submitted that "realistic time" was used and explained in the Specification (page 11, line 27 to page 12 line 11). However, to claim in the alternative language, the term "realistic time" no longer exists in the claims. Therefore, withdrawal of the 112-rejection is respectfully requested.

CLAIM REJECTIONS UNDER 35 U.S.C. § 103 – Hughes and Frank

In paragraphs 5 and 6, claims 1-2, 5, 13-14, 17, 23-24, 27 and 33-35 were rejected under 35 U.S.C. § 103 (a) as being unpatentable by U.S. patent number 5,784,582 to Hughes ("Hughes") and U.S patent number 5,297,265 to Frank ("Frank"). The rejection is traversed. Hughes and Frank, either alone or in combination, do not teach every elements of the claimed invention. The alleged motivation for combing Hughes and Frank is improper. Showing of the prima facie case for obviousness failed.

The Final Office Action re-asserted the assertion in the First Office Action that "Hughes discloses a system and method for managing access latency by *prioritizing memory access requests* among a plurality of data paths based on configuration parameters, wherein the configuration parameters comprise location, size and direction of the transfer in combination with information of the current request" (emphasis added). As presented in the Amendment ("first Amendment") in response to the First Office Action, and it is respectfully re-submitted that, while the First and Final Office Action's assertion is true, Hughes does not teach elements of the claimed invention.

Regarding claims 1 (and 2, 5, 23-24, 27, 33, and 35), the Final Office Action asserted:

> Hughes teaches the system and method substantially as claimed comprising the steps of: upon accessing the memory system for a piece of data used by a first process [i.e., request] determining an access time to acquire the piece of data in the memory system; comparing the determined access time to a threshold [i.e., comparing the size and location of the request to determine the time it takes to process the request and prioritize the request accordingly (Figure 3; column 5, lines 46-48); and taking actions based on the results of the comparing step; wherein a value of the threshold is selected based on whether the value is a realistic time for a memory access [Due to 112 rejection above with regarding to the limitation of 'realistic time', Examiner is hereby interpret 'realistic time' as being a function of size, location, and/or direction; Hughes teaches that the requests are being prioritized according to its size, location, and direction (Figure 4; column 2, lines 10-43]; column5, line 63 through column 6, line 5; and column 6, lines 46-49].

The Final Office Action failed to show correspondence between the teaching of Hughes and the claim limitations. The Office Action corresponded the whole phrase of the claimed text "upon accessing the memory system for a piece of data used by a first process" to only one word "request." It was not clear what "request" was corresponded to (e.g., accessing the memory system, a piece of data, or a first process).

Regardless of what "request" was corresponded to, as indicated in the First Amendment, and it is hereby re-submitted that claim 1 includes limitations comparing *an access time* to acquire a piece of data in the memory system *to a threshold* and *taking an action based on results of such comparison*. In contrast, Hughes is about *prioritizing the requests* for access to the shared memory system, which is patentably distinguished from the claimed invention. Hughes does not disclose the claimed "an access time to acquire a piece of data in the memory system," "a threshold," "comparing an access time . . . to a threshold," "taking an action based on results of the comparing step," etc.

The Final Office Action failed to show in Hughes the claimed limitation of "upon accessing the memory system for a piece of data used by a first process, determining an access time to acquire the piece of data in the memory system." While Hughes discloses "requests" for access to the shared memory, it does not teach, suggest, or make obvious the claimed "determining *an access time to acquire the piece of data* in the memory system" (emphasis added). Hughes' access to the shared memory system and/or requests for access to the shared memory does not teach the access time *to acquire* the piece of data or *determining* such access time.

The Final Office Action cited Hughes' Figure 3 and col. 5, lines 46-48 to correspond the claimed "comparing the determined access time to a threshold" to Hughes' "comparing the size and location of the request to determine the time it takes to process the request and prioritize the request accordingly." However, Hughes' cited Fig. 3 shows a block diagram of a shared memory arbiter/controller (col. 3, lines 42-43). Hughes' col. 5, lines 46-48 recite "[t]he request selection processor 108 is coupled to the control state registers 109 to provide parameters for the selection process." Both recitations of Hughes include the parameters for the *selection process of the request to access memory* and thus relate to the process of selecting the requests

to access memory but have no bearing on the claimed *access time, the threshold* or *comparing* the access time to the threshold, etc. Both recitations of Hughes do not disclose the Final Office Action's assertion's "comparing the size and location of the request to determine the time it takes to process the request and prioritize the request accordingly." As a result, both recitations do not teach the claimed elements. Even if the assertion of the Final Office Action is true, e.g., the comparison of the size and location of the request is to determine the time it takes to process the request and prioritize the request, the claimed access time is patentably distinguished from *the time it takes to process* the request and/or to *prioritize* the request in Hughes. The claimed access time relates to the time *to acquire* a piece of data in the memory system while Hughes' corresponded time does not relate to the time to acquire a piece of data in the memory system, but relates to the time it takes *to process the request for access* to the shared memory system or to prioritize such requests. Taking time *to acquire a piece of data* is far from patentably the same as taking time *to process the requests* for access to the memory system and/or to prioritize such requests. In brief, the Final Office Action failed to show at least the claimed "access time" "threshold," "determined access time," and "comparing the determined access time to a threshold."

The Final Office Action's interpretation of "realistic time" is traversed. However, because, to claim in the alternative language, the limitation related to "realistic time" is no longer in the claimed text. Therefore, additional discussion related to "realistic time" is no longer necessary.

It is not clear from the Final Office Action what in the cited Figure 4; column 2, lines 10-43; column 5, lines 63 through column 6, line 5; and column 6, lines 46-49 was corresponded to what elements in the claimed invention. Specific correspondence of the elements in Hughes to each of the claimed elements would be

very much appreciated. Further, for the rejection to sustain, correspondences in the prior art to the claimed elements must be shown.

Hughes' cited Fig. 4 is a flowchart illustrating the process executed in the shared memory arbiter (col. 3, lines 45-46) in which the controller receives multiple requests for access to the shared memory. If more than one request has the highest priority, then a process is executed to select the optimum request. However, if only one request has the highest priority, then the highest priority request is selected (col. 6, lines 63-66). Hughes' cited col. 2, lines 10-43 discloses a shared memory architecture based on the use of SRAM, which executes read, write and refresh requests for access to the memory in a pipeline fashion. In the shared memory architecture, a plurality of data paths is coupled to the shared memory which generates requests for access to the shared memory. The requests have characteristics including a starting address, a length and an access type, which are processed in a memory controller. In one aspect, the memory controller includes logic responsive to configuration parameters to control the data paths sharing the memory. The configuration parameters comprise a data path priority parameter to manage the latency of stored requests from the plurality of data paths. A data path can be given highest priority and be processed ahead of requests from other data paths, and thus provides protection to the high priority data path to ensure best case access to the shared memory. As can be seen, these cited paragraphs relate at best to the requests for memory access and prioritization of such requests, but have no bearing on the claimed invention including limitations such as an access time to acquire the piece of data in the memory system, a threshold, comparing the determined access time to a threshold, etc.

Hughes' cited column 5, line 63 through column 6, line 5 discloses that the request selection processor is able to select a request synchronously from each of the

buffers 104 through 107 to manage the shared memory pipeline. Further, the source of the data, the beginning address of the data, the size of the access and the direction of the access are all utilized in combination with information about current requests pending in the shared memory pipeline, in order to select a next optimum request according to parameters, etc. Hughes' cited column 6, line 46-49 discloses that the arbiter needs to consider the location, size and direction of the transfer to achieve the optimum arbitration decision along with the parameters of the current access. Again, these cited paragraphs have no bearing on the claimed invention including limitations such as an access time to acquire the piece of data in the memory system, comparing the determined access time to a threshold, etc.

The Final Office Action then conceded:

> However, Hughes does not specifically teach using a memory table having entries to convert a location address corresponding to an entry pointing to the location of the piece of access data, wherein the memory table working with a memory manger managing the data blocks independent of an operating system working with the memory system and independent of a processor working with the memory system.

and concluded

> Frank teaches a system and method for using a memory table [i.e. cache directory] to convert a location address corresponding to an entry pointing to the location of the piece of access data [see Figure 5 and column 11, line 23 through column 12, line 68]. Accordingly, it would have been obvious for one skilled in the art at the time the invention was made to implement the system and method for managing a memory system as taught by Hughes and to utilize a memory table as taught by Frank to improve data coherency, which requires little or no software overhead, as well as reducing memory access latency and bus contention providing a multiprocessing system with unlimited scalability as pointed out by Frank on column 2, line 27 through line 37.

However, Frank does not provide the limitations discussed above and not taught in Hughes, and the alleged motivation for combining the teachings of Hughes and Frank is improper. Therefore, the claimed invention is patentably distinguished

from Hughes and Frank, either alone or in combination. For example, Frank does not disclose the claimed "determining an access time to acquire the piece of data in the memory system" "comparing the determined access time to a threshold" and "taking an action based on results of the comparing step."

Even if Frank discloses a memory table that converts a location address corresponding to an entry pointing to the location of the piece of access data as asserted by the Final Office Action, this teaching of Frank is irrelevant to claim 1 because claim 1 does not include such limitations. In another word, this teaching of Frank does not correspond to the claim elements of claim 1.

Frank's cited figure 5 depicts an "interrelationship between system virtual addresses, descriptors, and cache directories (column 5, lines 17-19). Frank's cited paragraph column 11, line 23 through column 12, line 68 discloses the memory system stores data in units of pages and subpages. The memory system can handle address space management. The processor communicates with the memory system via two logical interfaces, e.g., the data access interface and the control access. The association between cache pages and SVA pages are recorded by each cache in its cache directory. Each cache directory is made up of descriptors. Each cache directory acts as a content-addressable memory. As can be seen Frank's cache directory is patentably distinguished from the claimed memory table including entries that point to data blocks and that are used to locate data in the data blocks. There is no specific showing of what in Frank corresponds to the claimed "memory manger", "the memory table working with the memory manger managing the data blocks" and such management is "independent of an operating system working with the memory system and independence of a processor working with the memory system" while the first process is being executed. It is respectfully submitted that Frank does not teach the claimed memory manager; Frank does not teach "the memory table working with

the memory manager managing the data blocks;" Frank does not teach such management of the data blocks is "independent of an operating system working with the memory system and independent of a processor working with the memory system" while the first process is being executed. Showing of those teachings in Frank is invited.

The assertion that "it would have been obvious . . . to implement the system and method for managing a memory system as taught by Hughes and to utilize a memory table as taught by Frank to improve data coherency, which requires little or no software overhead, as well as reducing memory access latency and bus contention providing a multiprocessing system with unlimited scalability as pointed out by Frank on column 2, line 27 through line 37" is improper because it is merely a broad conclusory statement and no evidence that suggests the combination of Hughes and Franks was provided. The assertion is a recitation of Frank that does not suggest the motivation for combining the teaching of Hughes and Frank. Therefore, the alleged motivation is insufficient to support a prima facie case of obviousness.

Because Hughes and Frank, either alone or in combination, do not teach, suggest, or make obvious every elements of claim 1, claim 1 is patentable.

Claims 2, 5 and 33, depending from claim 1, are patentable for at least the same reasons as claim 1. Claims 2, 5, and 33 are also patentable for their additional limitations that are not taught in Hughes or Frank, such as the data block containing the piece of data is placed in the memory system based on information selected in one or a combination of a movement pattern of data in the data block, a structure of the memory system, and a cache-level architecture in the memory system, the memory table using a physical address of a memory page corresponding to the piece of data to convert to a location address corresponding to an entry pointing to the location of the piece of data.

Claims 13, 14, 17 and 34 and 23, 24, 27, and 35 recite limitations corresponding to claims 1, 2, 5, and 33, respectively, and are therefore patentable for at least the same reasons as claims 1, 2, 5, and 33.

Regarding claims 13-14, 17 and 34, the Final Office Action re-asserted the assertion in the First Office Action that "Hughes teaches a computer implemented process" without providing evidence, and the assertion is therefore improper. Further, the assertion that it is inherent that "the program accomplishing the procedures must be carried or stored on a computer medium" is also improper because the mere fact that a certain result or characteristic may occur or be present in the prior art is not sufficient to establish inherency. The Final Office Action failed to rebut the argument in the First Amendment.

CLAIM REJECTIONS UNDER 35 U.S.C. § 103 – Lamberts and Eickemeyer

In paragraph 7, claims 6-8, 11, 18-19, 21, 28-29, and 31 were rejected under 35 U.S.C. 103(a) as being unpatentable over Lamberts and U.S. patent number 6,049,867) to Eickemeyer ("Eickemeyer"). The rejection is traversed. Lamberts and Eickemeyer, either alone or in combination, do not teach every elements of the claimed invention. The alleged motivation for combining Lamberts and Eickemeyer is improper. Showing a prima facie case of obviousness failed.

Regarding claims 6-8, 11, 28-29, and 31 the Final Office Action cited Lamberts' Figure 3 and Figure 4. The Office Action also corresponded the claimed "comparing the time taken to complete the memory access to a threshold" to "determining whether to overwrite data based on the estimated access time." The Final Office Action failed to correspondence elements in Lamberts to the claimed "the time taken to complete the memory" and "a threshold." If Lamberts' "estimated access time" is corresponded to the claimed "time taken to complete the memory

access," then Lamberts' estimated access time is used to determine whether to overwrite data, but such estimated access time is not compared to a threshold and taking an action based on such comparison as in the claimed invention. If Lamberts' "estimated access time" is corresponded to the claimed "threshold," then there is no correspondence to the claimed "time taken to complete the memory." Further, comparing the time taken to complete the memory access (to a threshold) of the claimed invention is far from patentably the same as determining whether to overwrite the data in Lamberts. There is no teaching in Lambert regarding "determining" that corresponds to the claimed "comparing."

Lamberts' figures 3 and 4 disclose the cache management method for processing write and read commands, respectively, but do not teach, suggest, or make obvious a threshold, the time taken to complete the memory access, or comparing such time to such threshold. The claimed "taking an action" is "based on results of the *comparing step*" (emphasis added). Since Lamberts does not disclose the step of comparing the time taken to complete the memory access, Lamberts cannot disclose taking an action based on results of such comparison.

The Final Office Action's interpretation of "realistic time" is traversed. However, because, to claim in the alternative language, the limitation related to "realistic time" is no longer in the claimed text. Therefore, additional discussion related to "realistic time" is no longer necessary.

The cited FIG. 3, references 64, 68, 70, and 72 are about writing data block to disk if the data block has the lowest cost function, overwriting cached read data with new data block if the read command type has the lowest cost function and writing cached write data to disk and overwriting cached write data block with new data block if the write command type has the lowest cost function. The cited FIG. 4, references 96, 100, 102, and 104 are about not storing the data block in cache if the data block

has the lowest cost function and overwriting cached read data with new data block if the read command type has the lowest cost function, writing cached write data to disk and overwriting cached write data with new data block if the write command type has the lowest cost function. The cited col. 4 lines 29-55 disclose managing a cache based on the access time of the command under consideration wherein if a data block has a higher access time, it is preferably kept or added into cache while data with a lower access time is preferably not stored in cache. As presented in the First Amendment, and it is hereby re-submitted that these cited references of Lamberts do not disclose determining an access time to acquire the piece of data in the memory system. These cited references do not disclose a threshold. As a result, these cited paragraphs cannot logically disclose comparing the determined access time to the threshold.

Both the First Office Action and the Final Office Action admitted that Lamberts does not specifically teach the claimed element of "accessing the memory system for a piece of data used by the first process, a processor working with the memory system continuing its function until it is *stalled*" (emphasis added). Both the First and Final Office Action then asserted "Eickemeyer teaches a system and method for memory management to reducing memory access latency utilizing a process or thread switch to allow the switching between multiple threads in response to the occurrence of an event such as a cache miss or stall that indicates long memory latency may occur. In an event of a cache miss, a first thread is suspended allowing a second thread to access the cache memory."

However, no evidence was provided to show that Eickemeyer provides the limitation of a processor working with the memory system continuing its function until it is *stalled* that is not taught in Lamberts. The cited Abstract of Eickemeyer discusses terminating the first thread, selecting a second thread in response to a level two or higher cache miss. Eickemeyer's cited paragraph of column 4, lines 27-55

discusses switching between multiple threads in response to the occurrence of an event which indicates long memory latency may occur or in response to events which will take a longer period of time to complete than is required to refill the instruction pipeline. Eickemeyer's cited paragraph of column 5, lines 4-7 discusses when a first thread is suspended in response to the occurrence of a level two cache miss a second thread would be able to access the level two cache for data presented therein. However, none of the citations discloses anything related to a processor continuing its *function until it is stalled* as asserted by both the First and Final Office Action. As a result, Lamberts and Eickemeyer, either alone or in combination, do not teach every elements of the claimed invention.

The alleged motivation for combining Lamberts and Eickemeyer is improper because the assertion that "the utilization of a process switch provides further memory access latency reduction and eliminates the need for complex, replication of pipeline latches and pipeline states rendering a cost effective system" is conclusory without specificity related to Lamberts. This assertion, if any, is utilized by Eickemeyer, but does not suggest the motivation for combining the two teachings of Lamberts and Eickemeyer. Therefore, a prima facie case of obviousness for combining the two teachings failed.

For the foregoing reasons, claim 6 is patentable. Claims 7-10 depend from claim 6 and are therefore patentable for at least the same reasons as claim 6. Claims 7-10 are also patentable for their additional limitations. For example, regarding claim 7, even though Eickemeyer discusses switching between multiple threads, as discussed, the alleged motivation for combination failed. Further, Eickemeyer does not teach switching the processes in the context of other limitations in claim 6. Additionally, both Lamberts and Eickemeyer do not disclose causing a performance monitor on the memory system or on a system using the memory subsystem.

Regarding claims 8 both Lamberts and Eickemeyer do not disclose a latency manager being part of managing the memory system. Both Lamberts and Eickemeyer do not disclose polling the latency manager for the time taken to complete the memory access.

Claims 18, 19 and 20 and 28, 29, and 30 recite limitations corresponding to claims 6, 8, and 9, respectively, and are therefore patentable for at least the same reasons as claims 6, 8, and 9, respectively.

Regarding claims 11, 21 and 31, both Lamberts and Eickemeyer do not disclose the additional limitation "counting a time elapsed from the time the data access starts; the counted time being increased as the data is being accessed." Other limitations in these claims are not disclosed in Lamberts as discussed above. They are not disclosed in Eickemeyer, either. Therefore, claims 11, 21, and 31 are patentable. Claims 12, 22, and 32 depend from claims 11, 21, and 31, respectively, and are therefore patentable for at least the same reasons as claims 11, 21, and 31. Claims 12, 22, and 32 are also patentable for their additional limitations.

Regarding claims 18-19 and 21, the Office Action asserted that "Lamberts teaches a computer implemented process" without providing evidence, and the assertion is therefore improper. The assertion that it is inherent that "the program accomplishing the procedures must be carried or stored on a computer medium" is also improper because the mere fact that a certain result or characteristic may occur or be present in the prior art is not sufficient to establish inherency.

CLAIM REJECTIONS UNDER 35 U.S.C. § 103 – Lamberts, Eickemeyer and Frank

In paragraph 8, claims 9-10, 12, 20, 22, 30, and 32 were rejected under 35 U.S.C 103(a) as being unpatentable over Lamberts and Eickemeyer as applied to claim 6, 11, 18, 21, 28 and 31, and further in view of Frank. The alleged motivation

for combining Lamberts, Eickemeyer, and Frank is improper. Lamberts, Eickemeyer, and Frank, either alone or in combination, do not provide the claimed limitations. Showing a prima facie case of obviousness failed. As discussed above, the alleged motivation for combining the teaching of Lamberts and Eickemeyer was improper. The alleged motivation for combining Frank was also improper. Showing a prima facie case of obviousness failed.

Regarding claims 9-10, 12, 30 and 32, the Final Office Action conceded that "neither Lamberts nor Eickemeyer teaches the usage of a memory table having entries to convert a location address corresponding to an entry pointing to the location of the piece of access data, wherein, while the first process is being executed, the memory table working with a memory manager managing the data blocks independent of an operating system working with the memory system and independent of a processor working with the memory system."

Frank does not provide the claimed elements that were not taught in Lamberts and Eickemeyer. Further, as discussed above, Frank's cache directory is patentably distinguished from the claimed memory table including entries that point to data blocks and that are used to locate data in the data blocks. Frank does not disclose the claimed memory manager. Frank does not disclose "the memory table working with the memory manager managing the data blocks." Frank does not disclose such management of the data blocks is "independent of an operating system working with the memory system and independent of a processor working with the memory system" while the first process is being executed. As a result, Lamberts, Eickemeyer, and Frank, either alone or in combination, do not teach every elements of the claimed invention. Further, showing a prima facie case of obviousness failed.

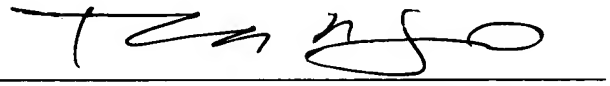
Regarding claims 20 and 22, the Office Action asserted that "Lamberts teaches a computer implemented process" without providing evidence, and the assertion is

therefore improper. The assertion that it is inherent that "the program accomplishing the procedures must be carried or stored on a computer medium" is also improper because the mere fact that a certain result or characteristic may occur or be present in the prior art is not sufficient to establish inherency.

SUMMARY

In conclusion, claims presented for examination clearly present subject matter that is patentable over the prior art of record, and therefore withdrawal of the rejections and issuance of the application is respectfully requested.

Respectfully submitted,

Date: Dec 16, 2004 By: 

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